REMARKS

Claims 1, 3, 5-8, 10 and 12-14 are pending in the present application. Claims 1 and 8 have been amended. Claims 15, 17 and 19-21 have been canceled.

Claim Rejections – 35 U.S.C. 102

Claims 1, 3, 5, 6, 8, 10, 12, 13, 15, 17, 19 and 20 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Brunolli et al. reference (U.S. Patent No. 6,201,491). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The digital-to-analog converting circuit of claim 1 includes in combination a first potential terminal; a second potential terminal; an output node; a first resistor circuit; a first switching circuit "including P-channel type MOS transistors, each of the P-channel type MOS transistors connected directly to first potential terminal, and to respective ones of the first connecting points and the first node, wherein only the P-channel type MOS transistors are connected to the first resistors as switches"; a second resistor circuit; a second switching circuit "including N-channel type MOS transistors, each of the N-channel type MOS transistors connected directly to the second potential terminal, and to respective ones of the second connecting points and the second node, wherein only the N-channel type MOS transistors are connected to the second resistors as switches"; and a control circuit. Applicant respectfully submits that the Brunolli et al. reference as relied upon does not disclose these features.

The Examiner has interpreted switches S_9 through S_{12} in Fig. 3 of the Brunolli et al. reference as the first switching circuit of claim 1, and switches S_1 through S_4 as the second switching circuit of claim 1.

However, as described in column 3, lines 3-6 of the Brunolli et al. reference, an embodiment of the digital potentiometer may be fabricated on an integrated circuit die using complimentary metal oxide semiconductor (CMOS) transistors for the switches. This would mean that switch S_{11} in Fig. 3 of the Brunolli et al. reference for example, would include a pair of coupled PMOS and NMOS transistors connected at one end to Vcc and connected at the other end to the node between resistors R_{LSB}. Each of switches S_1 through S_{12} would be configured in a somewhat similar manner.

Since each of switches S_9 through S_{12} in Fig. 3 of the Brunolli et al. reference are CMOS switches that include both PMOS and NMOS transistors, switches S_9 through S_{12} cannot be interpreted as the first switching circuit of claim 1, which is featured as "including P-channel type MOS transistors, each of the P-channel type MOS transistors connected directly to first potential terminal, and to respective ones of the first connecting points and the first node, wherein only the P-channel type MOS transistors are connected to the first resistors as switches", as would be necessary to meet the features of claim 1. For somewhat similar reasons, switches S_1 through S_4 in Fig. 3 of the Brunolli et al. reference cannot be interpreted as the second switching circuit of claim 1. Applicant therefore respectfully submits that the digital-to-analog converting circuit of claim 1 distinguishes over the Brunolli et al. reference as relied upon, and that

this rejection, insofar as it may pertain to claims 1, 3 and 5-7, is improper for at least these reasons.

The digital-to-analog converting circuit of claim 8 includes in combination a plurality of first switches "each of which is connected directly to the first potential terminal, and to respective ones of the first connecting points and the first node, wherein only P-channel type MOS transistors are connected to the first resistors as switches"; and a plurality of second switches "each of which is connected directly to the second potential terminal, and to respective ones of the second connecting points and the second node, wherein only N-channel type MOS transistors are connected to the second resistors as switches".

For at least somewhat similar reasons as set forth above, switches S_9 through S_{12} in Fig. 3 of the Brunolli et al. reference cannot be interpreted as the first switches of claim 8, because each of CMOS switches S_9 through S_{12} in Fig. 3 include both PMOS and NMOS transistors. That is, the Fig. 3 embodiment of the Brunolli et al. reference does not include only P-channel type MOS transistors connected to first resistors as switches. Likewise, CMOS switches S_1 through S_4 cannot be interpreted as the plurality of second switches of claim 8. Applicant therefore respectfully submits that the digital-to-analog converting circuit of claim 8 distinguishes over the Brunolli et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 8, 10 and 12-14, is improper for at least these reasons.

Claim Rejections – 35 U.S.C. 103

Claims 7, 14 and 21 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Brunolli et al. reference in view of the Leung et al. reference (U.S. Patent No. 6,400,300). Applicant respectfully submits that the Leung et al. reference as secondarily relied upon does not overcome the above noted deficiencies of the Brunolli et al. reference. Applicant therefore respectfully submits that claims 7 and 14 would not have been obvious in view of the prior art as relied upon by the Examiner for at least these reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

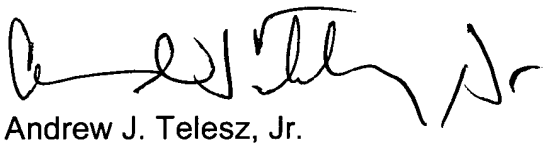
In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of one (1) month to July 31, 2006, for the period in which to file a response to the outstanding Office Action. The required fee of $120.00 should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



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